

Ten Tips to Improve an IC Design Teams Project Execution

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Chandler, AZ (PRWEB) April 9, 2006 — Many IC design projects are frequently struggling with unexpected delays to their production plan. Intense time to market pressures demands an environment that prescribes improvement to both the predictability and length of design timelines. In consideration of this continuous improvement aspiration Jorvig Consulting has compiled ten vital tips for consideration as teams pursue their quest to improve IC design execution.

- 1) Identify and close any Tool gaps. – In many cases design engineers will do what they do best and engineer a unique solution to their tool problem. The solution for each engineer will likely be different, creating potential integration issues as all the lower level pieces come together. Identify tool issues and/or gaps and make their resolution part of the project plan. Closure on unresolved tool issues will minimize integration rework and eliminate the wasted, unplanned engineering time spent on multiple solutions to the same problem.
- 2) Find what is not known. – This item is ambiguous but essential. Many disconnects that prevent the desired crisp execution of a task are not necessarily obvious to the majority of the team. They must be hunted down, found and repaired. Engineers frequently deal with such items quietly, without much fanfare hence they will be subtle and elusive to discover.
- 3) Ensure who, what, where, how and when is defined for all tasks. – Most organizations handle the who and when part well since it fits nicely into a project management tool. What, where and how requires additional planning, reviewing and documentation to ensure proper alignment of deliverable and receivable expectations for all tasks. Surprises will erode your schedule without this critical alignment in place.
- 4) Large group task breakdown to identify design activities. – The identification of tasks to be planned and managed is best accomplished in a large group setting. This facilitates essential discussion, tradeoffs, team alignment and most importantly minimizes the possibility of missing a task in the plan.
- 5) Formalize the process for changes to scope. – Scope changes are a subtle, behind the scenes consumer of resources when not managed well. There must be a formal process in place for assessing a change and communicating the outcome to the design team with absolute clarity. Allowing designers to make assumptions about features will stimulate unpredictability in your plan.
- 6) Manage closure and content of the requirements. – The requirements can drag on for as long as the project takes to design it, when not managed well. This includes the engineering requirements for the internal blocks as well as the chip specification. Defining the scope of content is especially critical for the internal requirements. For these documents it is suggested content that includes what, how and where information as outlined in tip #3.
- 7) Specify design review requirements and adhere to them. – Think of design review requirements as a means of defining the design validation requisites. The review is the final stamp of approval indicating that

everything that should be done, has been done. Spelling out the requirements for the review ensures alignment on all design validation expectations across the team. Be sure to include the needs of product and test engineering in your review requirements to promote awareness of their needs for success.

8) Document & review design assumptions. – This is essentially an implementation plan and includes information that is typically not found in electrical specifications. For instance die sizes, resource plans, any optional FAB layers, baseline FAB processes, reuse plans and patent plans are examples of such additional information. It may also be beneficial to include schedule vs. feature vs. risk tradeoffs here to highlight those possibilities for the business.

9) Include product & test requirements as design requisites and manage closure. - Any requirements of the design in support of volume production must be addressed. If these items are skimped upon in the interest of making a sample date, there will be added risk of an all layer spin to implement them later. ESD, latchup, test modes, margin simulations and testability are examples of typical expectations that test and product engineering would request of design. These should be added to the design assumptions noted in tip #8.

10) Initial silicon evaluation must include any production margin limiters such as voltage, temp, ESD & latchup. – Fixes for these items along with any other functional fixes must be implemented together to avoid an additional all layer spin later, which is targeted only for improving production margin.

About Jorvig Consulting, Inc.

Jorvig Consulting provides services to enhance product design team execution. The solutions jointly developed with our clients enable design teams to experience a newfound freedom from surprises during project execution. The business result is a predictable design project that enables the business objectives.
<http://www.jorvigconsulting.com>

Contact Information: Jeff Jorvig at 480-895-0478

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Jeff Jorvig

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480-895-0478