



PIEmatrix as an online Design Guide for the NPD Process

**Advancing the Design Guide
Concept**



Introduction to Jorvig Consulting

New Product Development Process Consulting Services for the Semiconductor Industry

**Working with Clients to Enable a more Streamlined and
Predictable Path to New Product Revenue**

**Freedom from
Surprises!**

© Jeff Jorvig - Jorvig Consulting Inc.

December 18, 2008



Introduction to PIEmatrix



Process Management & Governance Company

Online framework for creating, implementing, and reusing best practices

© Copyright 2007 PIEmatrix Patent Pending US60/846,517

**Freedom from
Surprises!**

© Jeff Jorvig - Jorvig Consulting Inc.

December 18, 2008

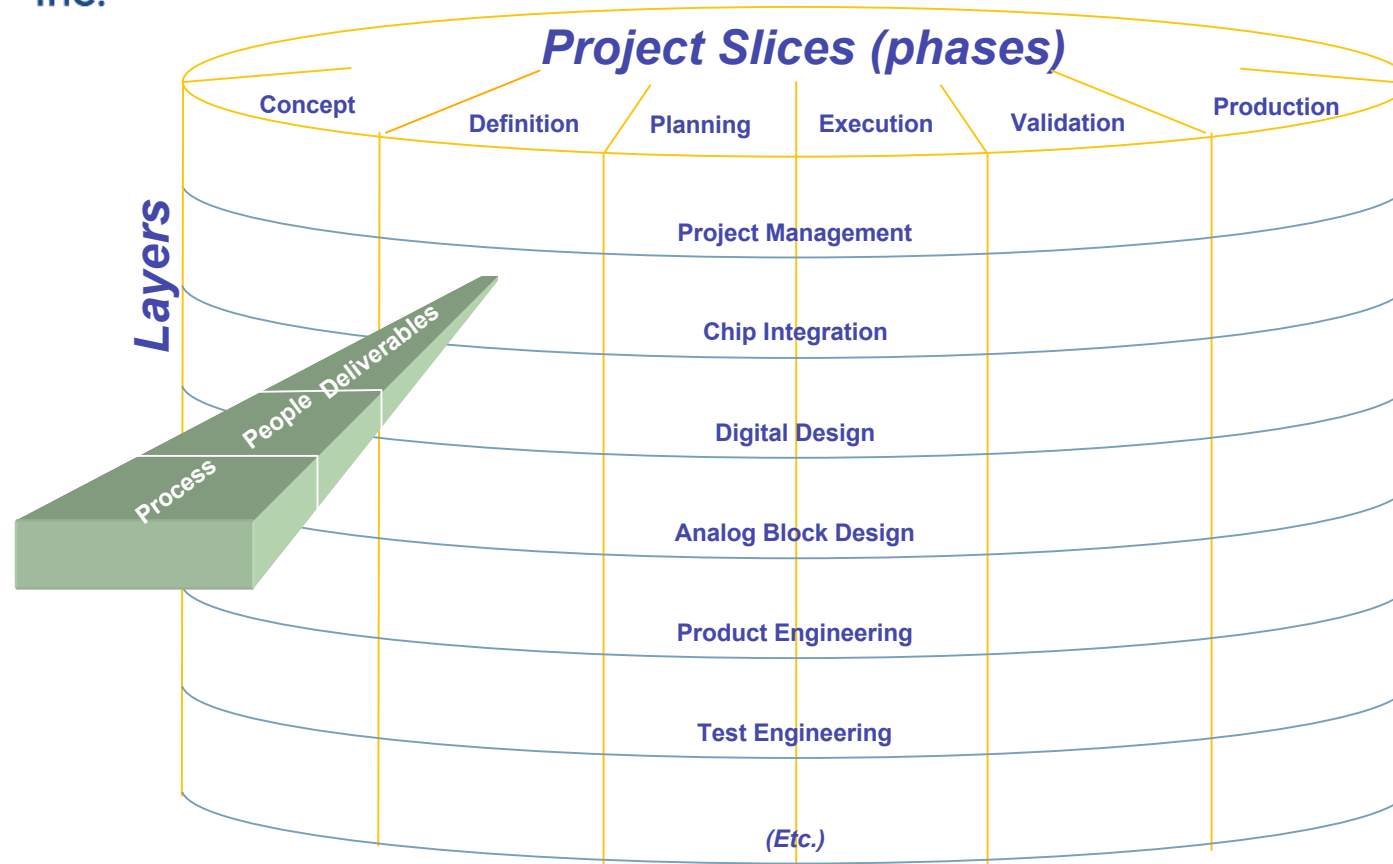


PIEmatrix: An Online Approach to Design Guides

- **A design guide document captures the order, procedures and data for a development project.**
 - This tends to be a shared file via email or on a server.
- **PIEmatrix can capture the procedures, resources, status and supporting data in a web based collaborative environment.**
 - PIEmatrix becomes an online design guide.
 - Easily updated and immediately visible to everyone.

**Freedom from
Surprises!**

PIEmatrix: Slices & Layers Concept for a Project



Each layer is a design guide for each functional area.

**Freedom from
Surprises!**

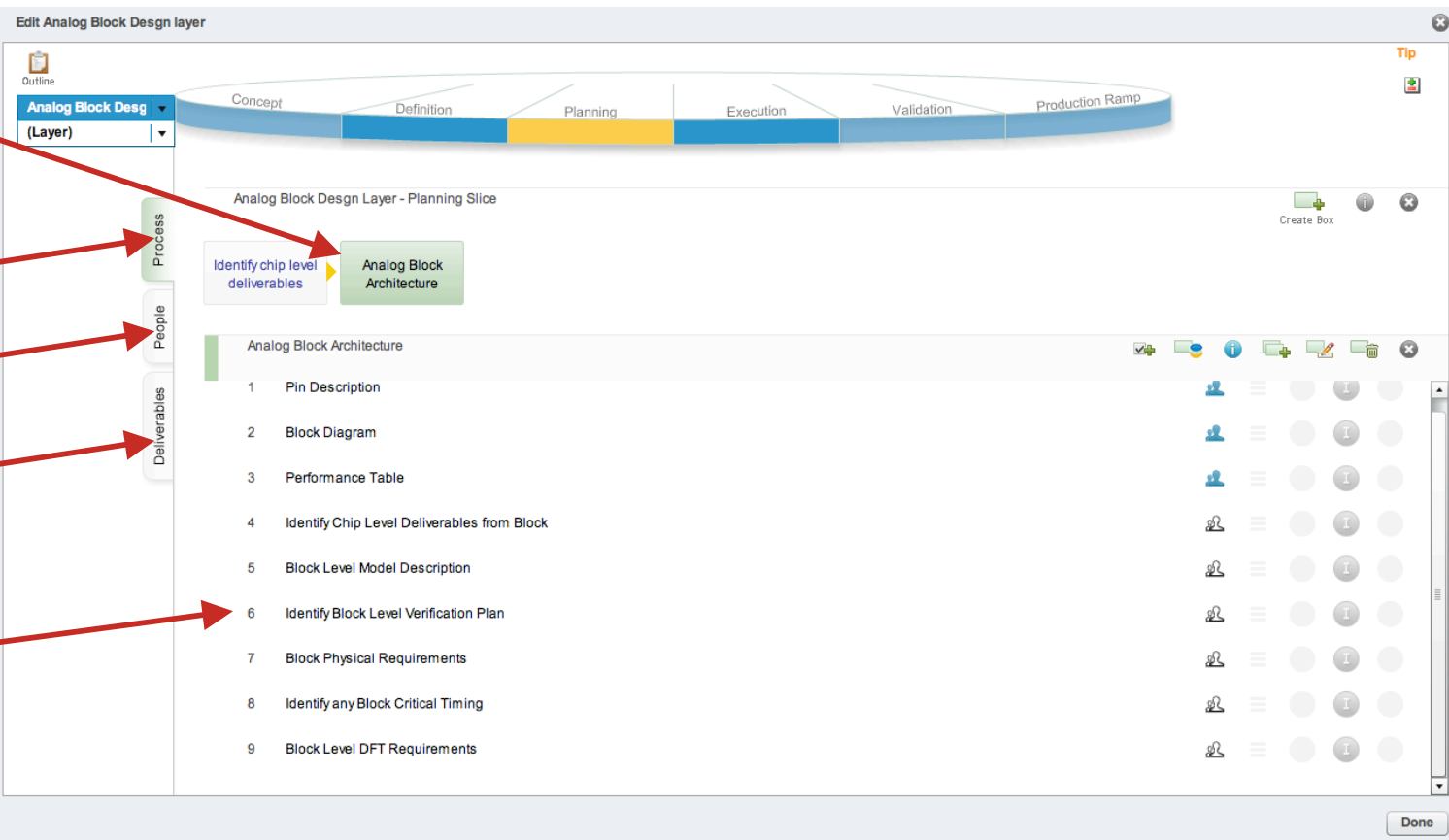


PIEmatrix Start Page

The screenshot shows the PIEmatrix interface. At the top right, there are links for 'PIEmatrix BETA', 'PIE Lobby', 'Help', and 'Exit Platform'. Below this is a navigation bar with 'Home', 'Project', 'To Do', and 'Dashboard' tabs. The user 'Jeff Jorvig' is logged in for 'Jorvig Consulting, Inc.'. On the left is a sidebar with categories: 'Current Projects', 'Archived Projects', 'Best Practices', 'Layers', 'Project Templates', 'Slice Sets', and 'Global Roles'. The main content area is titled 'Current Projects' and shows a project named 'IC Development'. A 'Public Tags' section shows '(None selected)'. A 'Tip' icon and a 'Create Project' button are also visible. Red arrows point from text labels on the right to specific elements in the interface: 'Project List' points to 'IC Development', 'Layer Setup View' points to 'Layers', 'Project Template View' points to 'Project Templates', 'Slices (phases) View' points to 'Slice Sets', and 'Resources View' points to 'Global Roles'.

Freedom from Surprises!

Analog Block Layer Edit View



The screenshot shows the 'Edit Analog Block Design layer' window. At the top, a progress bar indicates stages: Concept, Definition, Planning (highlighted in yellow), Execution, Validation, and Production Ramp. Below this, the 'Analog Block Design Layer - Planning Slice' is shown, containing a task 'Identify chip level deliverables' and a sub-task 'Analog Block Architecture'. The 'Analog Block Architecture' sub-task is expanded to show a list of tasks: 1 Pin Description, 2 Block Diagram, 3 Performance Table, 4 Identify Chip Level Deliverables from Block, 5 Block Level Model Description, 6 Identify Block Level Verification Plan, 7 Block Physical Requirements, 8 Identify any Block Critical Timing, and 9 Block Level DFT Requirements. On the left, a sidebar contains 'Process', 'People', and 'Deliverables' sections. Red arrows point from text labels to these sections and the task list.

Major Process Group → Analog Block Desg (Layer)

All Tasks for group → Process

All People for group → People

All deliverables for group → Deliverables

All subtasks related to Major Process Group → 1 Pin Description, 2 Block Diagram, 3 Performance Table, 4 Identify Chip Level Deliverables from Block, 5 Block Level Model Description, 6 Identify Block Level Verification Plan, 7 Block Physical Requirements, 8 Identify any Block Critical Timing, 9 Block Level DFT Requirements

Freedom from Surprises!



Document Repository within Process Box

IC Development PIEmatrix BETA | PIE Lobby | Help | Exit Platform

Home Project To Do Dashboard Jeff Jorvig | Jorvig Consulting, Inc.

Analog Block Desg (Layer) Calendar | List

Concept Definition Planning Execution Validation Production Ramp

Analog Block Design Layer - Definition Slice Deliverables Create Box | Info | Close

Define analog requirements → Estimate effort (Power/size/time) → Analog Block Opportunity Assessment

Define analog requirements Info | Close

- Templates & Tools
- Analog_guide_client.doc
- Work In Progress
- bandgap_guide.doc
- bias_guide.doc
- Final Deliverables

Template Docs for a Given Process Block

Active Project Docs copied from template to WIP folder

Once completed, they are migrated to final docs

Check-In/Check-Out Managed

Freedom from Surprises!



Chip Project Update View

Selected Phase & layer View

Process group Status

Process group within layer

Process group view tabs

Task, people & deliverable details within process group

Individual task updates

Freedom from Surprises!

Project Update View for Analog Block

IC Development PIEmatrix BETA | [PIE Lobby](#) | [Help](#) | [Exit Platform](#)

Jeff Jorvig | Jorvig Consulting, Inc.

Home | **Project** | To Do | Dashboard


PM Chip

Analog Block Desg

Chip Design

Digital RTL Design

(Layer)



PM Chip Layer - Planning Slice Process

Determine Activity Sequencing → Identify Activity Resources → Conduct Qualitative Risk Analysis → Estimate Activity Durations → Identify Risk → Plan Risk Response → Plan Risk → Create Work Breakdown Structure → Develop Schedule

Analog Block Design Layer - Planning Slice Process

Identify chip level deliverables → Analog Block Architecture

Analog Block Architecture

1	Pin Description								
2	Block Diagram								
3	Performance Table								
4	Identify Chip Level Deliverables from Block								
5	Block Level Model Description								

Task Status Update

Task Resource Assignment

Freedom from Surprises!

© Jeff Jorvig - Jorvig Consulting Inc.

December 18, 2008

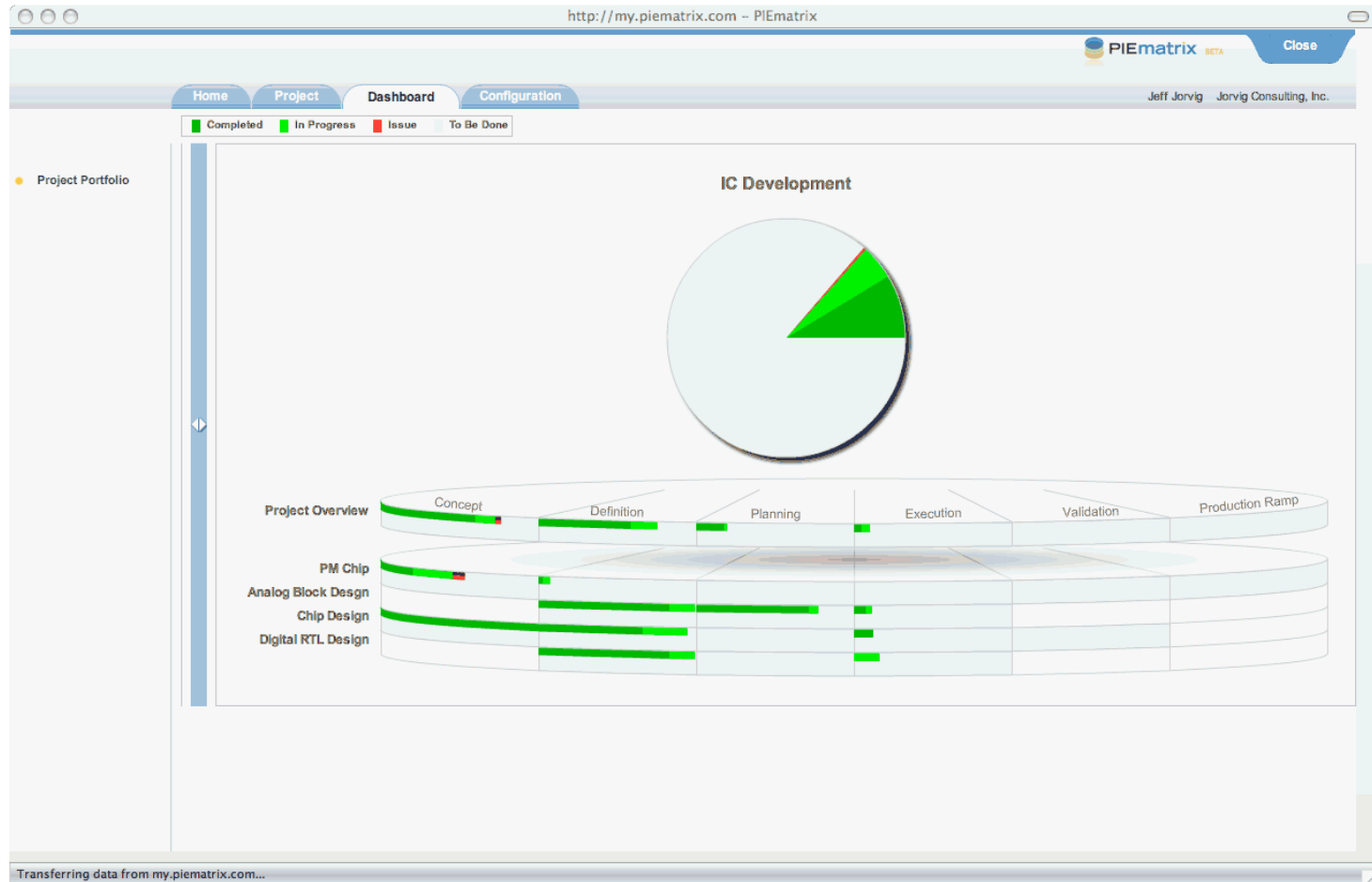


Project Status View

Dark green shows completion

Light green shows in progress

Red shows issues. Hover over for details



Freedom from Surprises!



Mapping Existing Design Guide to PIEmatrix

- **All activities would map into process groups along with related subtasks.**
 - Each functional area would be supported as a different layer: Analog design, digital design, layout, product engineering, test etc.
- **Data deliverables in the design guide would become deliverables for a process group within PIEmatrix.**
 - Templates for the data would be established in the process group repository.



Contact Information

Jeff Jorvig
480-895-0478
(Toll Free) 877-895-0478
jeff@jorvigconsulting.com
www.jorvigconsulting.com

**Freedom from
Surprises!**

© Jeff Jorvig - Jorvig Consulting Inc.

December 18, 2008